REMARKS

Claim Objections

Claims 14-25 and 29-39 are objected to as being unclear. Applicant appreciates the Examiner's suggestions and has adopted the suggested changes.

Claim Rejections under 35 USC §112

Claims 38-39 are rejected under 35 USC §112, first paragraph, as containing subject matter not described in the specification. Claim 38 has been amended to depend from claim 36, as intended, rather than claim 38. Applicant believes this amendment addresses the Examiner's concern.

Claim Rejections under 35 USC §103

Claims 14, 16-18, 20-22, 24-25 and 29-37 are rejected under 35 USC §103(a) as being unpatentable over Admitted Prior Art ("APA") in view of Nagamine (5,534,724) ("Nagamine") and Bothra et. al. (6,020,616) ("Bothra").

As to claims 14, 18, 22, 29, 33, 34, and 36, the Examiner states that the APA does not teach a substrate and plurality of dummy gates having a predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap, but that Nagamine discloses transistor gates of a predetermined width and length at a substantially identical gap and Bothra teaches dummy gates of predetermined width and length formed between and outside the adjacent transistors. Office Action, pages 5-6. The Examiner then states that it would have been obvious to combine the APA, Nagamine and Bothra to reduce inductive noise of the device.

The Examiner relies on Fig. 3 of Nagamine to support the obviousness rejection. Because the text supporting Fig. 3 fails to discuss an identical gap, Applicant assumes the Examiner is reading scale into Fig. 3. However, Fig. 3 does not support an identical gap. Rather, the gaps in Fig. 3 in Nagamine range from 0.8 to 1.1 cm. *See* Fig. 3. Moreoever, Bothra does not teach dummy gates of a predetermined width and length formed between and outside adjacent transistors. Rather, Bothra teaches dummy regions "substantially isolated" from active regions. Col. 8, lines 8-11. Therefore, neither invention nor the APA, alone or in combination, disclose Applicant's claims. As such, the claims and the claims which depend from them are patentable.

Claims 15, 19, and 23 are rejected under 35 USC §103(a) as being unpatentable over the APA, Nagamine and Bothra, and further in view of Hansch et. al. (6,174,741) ("Hansch"). The Examiner states that with respect to these claims, the APA, Nagamine and Bothra teach the claimed structure except that the length of the dummy gates is substantially the same as that of the transistor gates. Office Action, page 10. According to the Examiner, Figs. 3B and 4 of Hansch discloses this feature. The text of figure 4 states otherwise:

> The gate line (GL) is a substantially rectangular feature with a width (W) and a length (L). . . The first dummy gate line (DGL_1) is a substantially rectangular feature having a width (W) and a length (L_D). . . Similarly, the second dummy gate line (DGL_2) is a substantially rectangular feature having the width (W) and the length (L_D).

Col. 7, lines 34-48. Hansch explicitly distinguishes between the length of the gate (L) and the dummy (L_D). Hansch does not state these values are the same, rather the inference is the opposite. By adopting a different legend to describe the length of the dummy gate and keeping the same legend with respect to the width, the only conclusion one can reach is that the lengths are different. Therefore, Hansch teaches transistor gates and dummy gates of different lengths, which teaches away from Applicant's invention. Therefore, neither the APA or the cited references, alone or in combination, disclose Applicant's claims. As such, the claims and the claims which depend from them are patentable.

Claims 38-39 are rejected under 35 USC §103(a) as being unpatentable over APA, Nagamine and Bothra, and further in view of Neugebauer (5,748,835) ("Neugebauer"). Claim 38 has been amended to claim from 36, therefore the rejection is no longer applicable.

New claims 40-59 are directed to claims that are patentable over the APA and applied references. No new matter has been added.

For the foregoing reasons, reconsideration and allowance of all claims in the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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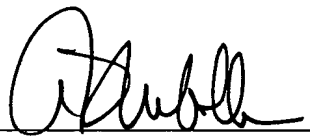

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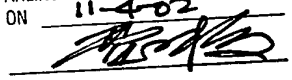

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

14. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially identical gap therebetween without intervening dummy gates therebetween [between ones of the adjacent transistor gates, without intervening transistor gates therebetween, on the substrate]; and

a plurality of dummy gates having predetermined width and length between ones of the adjacent transistors at a substantially identical gap therebetween, [between adjacent ones of the dummy gates, without intervening dummy gates therebetween, as that between the adjacent ones of the transistor gates on the substrate.] without intervening transistor gates therebetween, respectively.

18. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate is of predetermined width and length at a substantially identical gap therebetween without intervening dummy gates therebetween; [between adjacent ones of the transistor gates, without intervening transistor gates therebetween, on the substrate;] and

a plurality of dummy gates having predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap therebetween, [between adjacent ones of the dummy gates, without intervening dummy gates therebetween, as that between the adjacent ones of transistor gates on the substrate.] without intervening transistor gates therebetween, respectively.

22. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions of two or more adjacent transistors having at least more than one first and second electrodes disposed on the substrate;

a plurality of transistor gates disposed between more than one first and second electrodes of those active regions, the transistor gates being positioned such that at least more than one gate has a predetermined width and length at a substantially identical gap therebetween without intervening dummy gates therebetween; [between ones of the adjacent gates, without intervening transistor gates therebetween, on the substrate;] and

a plurality of dummy gates having predetermined width and length outside ones of the adjacent transistors at a substantially identical gap therebetween, [between adjacent ones of the dummy gates, without intervening dummy gates therebetween as that between the adjacent ones of the transistor gates on the substrate.] without intervening transistor gates therebetween, respectively.

29. (Twice Amended) A semiconductor device comprising:

a substrate;

active regions having a source region and a drain region on the substrate;

a portion other than the active region on the substrate;

a plurality of transistor gates formed on the active regions, the gates being disposed between the source region and the drain region and having a first gap between adjacent gates, without intervening [transistor] dummy gates therebetween;

a plurality of dummy gates formed on the portion, the dummy gates being characterized by a second gap between adjacent dummy gates, without intervening [dummy] transistor gates therebetween, respectively;

wherein the second gap is substantially identical to the first gap.

33. (Twice Amended) A semiconductor device comprising

a substrate;

a first region having a plurality of first active regions each having a source region and a drain region respectively and a first portion other than the plurality of first active regions on the substrate;

a second region having a plurality of second active regions each having a source region and a drain region respectively and a second portion other than the plurality of second active regions on the substrate;

a plurality of first transistor gates formed on the plurality of first active regions, disposed between the source region and the drain region, the plurality of first transistor gates being characterized by a first gap between neighboring transistor gates, without intervening transistor gates therebetween;

a plurality of second transistor gates formed on the plurality of second active regions, the plurality of second transistor gates also being characterized by the first gap between neighboring gates;

a plurality of first dummy gates formed on the first portion, the plurality of first dummy gates being characterized by a second gap between neighboring dummy gates, without intervening [dummy] transistor gates therebetween;

a plurality of second dummy gates formed on the second portion, the plurality of second dummy gates also being characterized by the second gap between neighboring dummy gates[;] without intervening transistor gates therebetween;

a first metal connected to the source and drain regions by a contact; and

a second metal connected to a first part of the first metal to supply a voltage.

39. (Amended) The semiconductor device according to claim [38] 36, in which adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates.

Claims 40-59 are new.